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Design of High Speed MAC Unit using Vedic Multiplier

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Abstract - The design of high speed MAC Unit using Vedic Multiplier is the techniques of Ancient Indian Vedic Mathematics that has been modified as per technology to improve performance of mathematically computational. MAC is used in DSP application to multiply and accumulate at the same time. Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculations based on 16 Sutras. The work has proved by the efficiency of Urdhva tirykbhyam Sutra and Nikhilam sutra– Vedic method for multiplication which strikes a difference in the actual process of multiplication itself and also reduces the complexity. It enables parallel generation of intermediate products, eliminates unwanted multiplication steps during the mechanism. For such application I used here carry select adder in the Vedic multiplier that has reduced the delay. Adders are the basic building blocks of any processor or data path application and computation. In adder design carry generation is the critical path. Carry Select Adder (CSLA) is one of the fast adder used in many data path applications. There is a chance to reduce the delay in the MAC structure.

Index Terms – MAC**,** Vedic Multiplier, Delay, Carry Select Adder, Urdhva Tirykbhyam, Delay.

1. INTRODUCTION

Multipliers and accumulators are widely used in Microprocessors, DSP and Communication applications and in such mathematic applications also for memory devices to storage data. For higher order multiplications, a huge number of adders are to be used to perform the partial product addition, that is too much complex. The need of low power and high speed Multiplier is increasing as the need of high speed processors are increasing in this age. The Vedic multiplication technique is based on 16 Vedic sutras or aphorisms, which are actually word formulae describing natural ways of solving a whole range of mathematical problems [1]. The mathematical operations using, Vedic Method are very fast and area efficient, this can be used to improve the computational speed of processors or any other application. This paper describes the design and implementation of 4x4 bit MAC unit using Vedic multiplier based on Urdhva-Tiryakbhyam sutra (Vertically and Crosswise technique) and Nikhilam sutra of Vedic Mathematics using EDA (Electronic Design Automation) tool. The paper is organized as follows-

Section 2 describes the basic methodology and algo of Vedic multiplication technique. Section 3 describes the proposed architecture of MAC unit using 2x2 and 4x4 bits Vedic Multiplier (VM) based on Vedic multiplication. The multiplier architecture can be generally classified into three categories. First is the serial multiplier which emphasizes on hardware and minimum amount of chip area. Second is parallel multiplier (array and tree) which carries out high speed mathematical operations. But the drawback is the relatively larger chip area consumption. Third is serial- parallel multiplier which serves as a good trade-off between the times consuming serial multiplier and the area consuming parallel multipliers [2] that is structured by using CSLA. Section 4 and 5 described the results of Vedic multiplier. And at last the comparison table and conclusion is described.

2. VEDIC MULTIPLIER AT A GLANCE

2.1 Basic principal-

High speed and high-throughput and reliable circuitry design are playing the challenging role for VLSI designer in the VLSI field. For real-time signal processing like DSP, a high speed and high throughput with good reliable MAC unit is always a key to achieve a high performance digital signal processing system and computational system [6].

2.2 Nikhilam sutra-

Nikhilam Sutra literally means “all from 9 and last digit from 10”. Although it is applicable to all cases of multiplication, it is more efficient when the numbers involved are large to reduce the complexity. Since it finds out the compliment of the large number from its nearest base to perform the multiplication operation on it, larger is the original number, lesser the complexity of the multiplication due to the compliment of the number. We first illustrate this Sutra by

considering the multiplication of two decimal numbers (92 * 89) where the chosen base is 100 which is nearest to and greater than both these two numbers [3].

STEP 1- Starts from left most digit and begin subtracting '9' from each of the digit but subtract '10' from the last digit.

- To multiply 92 & 89, apply Nikhilam Sutra-

92 ⇒ -08

89 ⇒ -11

STEP 2- multiply (-08) and(-11) to get 88.

92 ⇒ -08

x

89 ⇒ -11

88

STEP 3- Now we cross add.

92 -08

89 -11

STEP 4- In both operation we get the same answer. Which is written below-

92 ⇒ 08

x

89 ⇒ -11

81 88

2.3 Urdhva triyakbhyam-

The multiplier is based on an algorithm Urdhva Tiryakbhyam that is Vertical & Crosswise based principal of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication in mathematics. It literally means "Vertically and crosswise" [3]. It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The parallelism in generation of partial products and their summation is obtained using Urdhava Triyakbhyam explained in fig.[4].The algorithm can be generalized for n x n bit number.

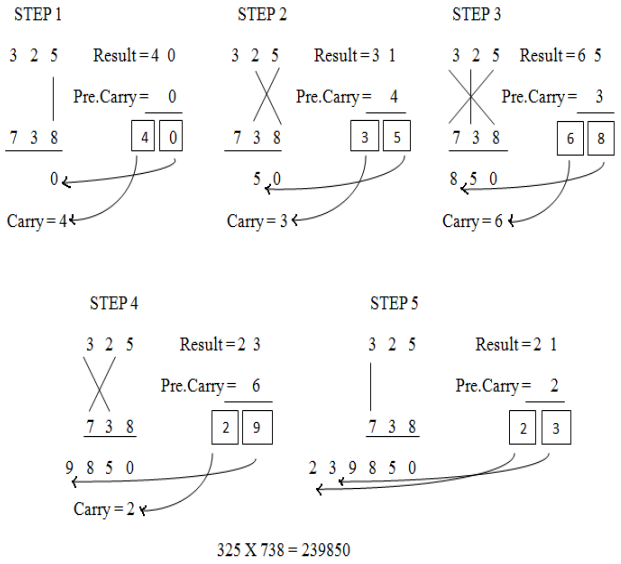

Fig.1: Multiplication by Urdhva Tiryakbhyam.[4]

3. PROPOSED MAC ARCHITECTURE

The hardware architecture of 2x2 and 4x4 bit Vedic multiplier (VM) modules are displayed in the below sections than there is used a carry select adder to reduced delay. Here, "Urdhva-Tiryakbhyam" (Vertically and Crosswise) & Nikhilam sutra is used to propose such an architecture for the multiplication of two binary numbers. And then there is use of adder and accumulator. The beauty of Vedic multiplier is that here partial product generation and additions are done concurrently as a parallel process. Hence, it is well adapted to parallel processing. The feature makes it more attractive for binary multiplications to reduce delay.

3.1 2X2 Multiplier-

This is fundamental block of 4X4 Vedic multiplier. Using four 2X2 multiplier we construct a 4X4 Vedic multiplier. The inner structure of 2X2 Vedic multiplier is as following [5]-

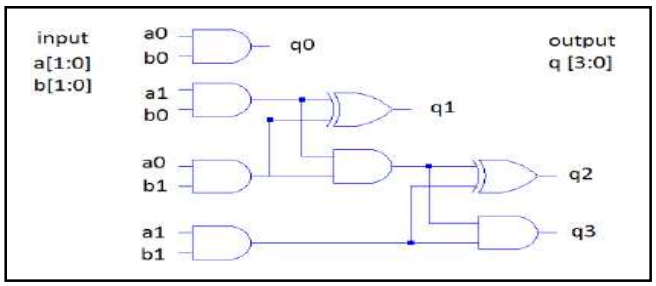

Fig 2 2X2 Vedic multiplier

3.2 Carry Select Adder-

Carry-Select adder is simple and area-efficient as well as reduced delay also a group of full adder. However, the computation speed is slow because each full-adder can only start operation till the previous carry-out signal is ready. In the carry select adder, N bits adder is divided into M parts. Each part of adder is composed two carry ripple adders with cin_0 and cin_1, respectively. Through the multiplexer, we can select the correct output result according to the logic state of carry-in signal [7].

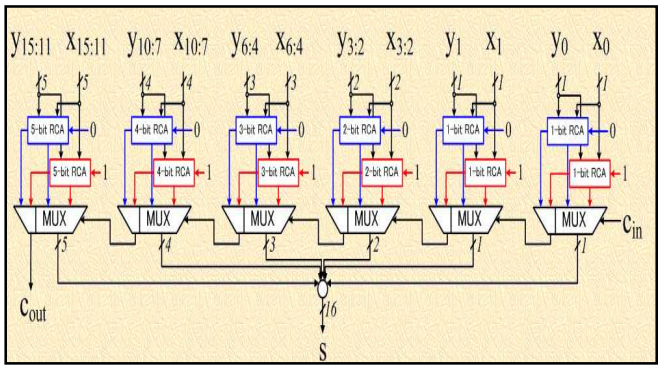

Fig 3 carry select adder[7]

3.3 MAC Unit using Vedic Multiplier—

The inputs for the MAC are fetched from memory location and fed to multiplier block of the MAC, which will perform multiplication and give the result to adder which will accumulate the result and then will store the result into a memory location; this is the overall process of MAC unit. This entire process is to be achieved in a single clock cycle [12]. The design of MAC unit architecture from Fig. shows that the design consists of one 8 bit register, one 4-bit Vedic multiplier, 8-bit accumulator using carry select adder (CSLA).

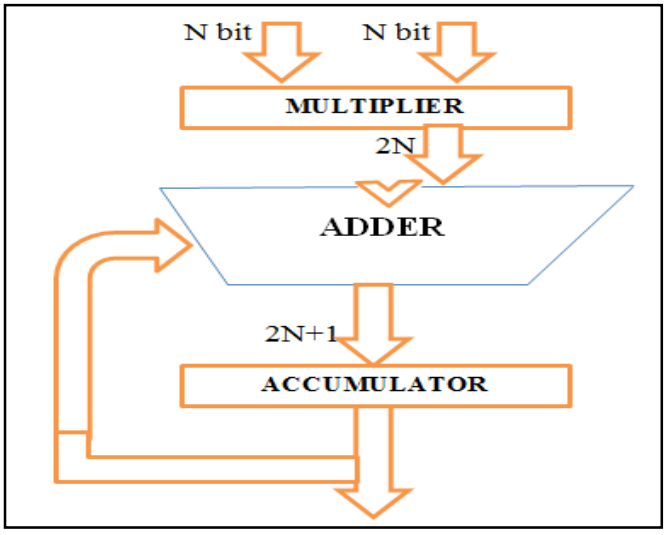

Figure 4: Structure for MAC Unit

A block diagram of 4X4 Vedic multiplier is given below-

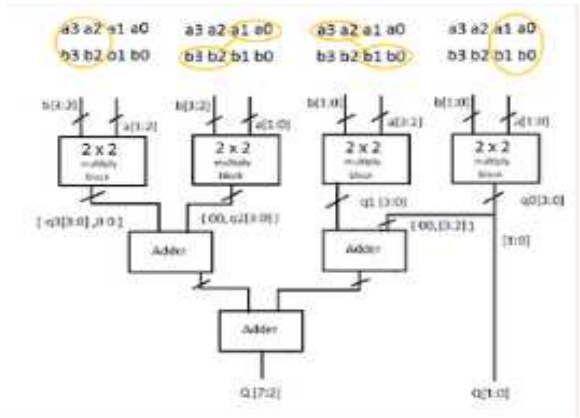

Fig.5 4X4 Vedic multiplier[9]

4. SIMULATION RESULT AND RTL VIEW

Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. The net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While a higher clock frequency generally results in increased processing power,

its disadvantage is that it also increases power dissipation which results in higher device operating temperatures.

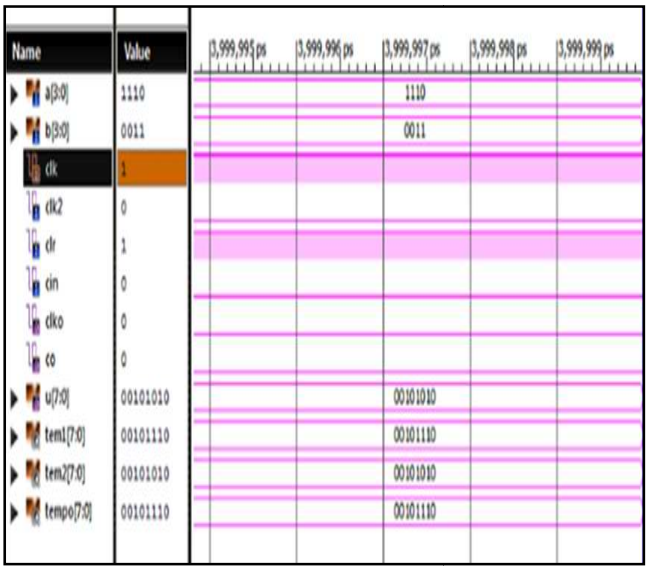

Fig.6 Simulation result of MAC Unit

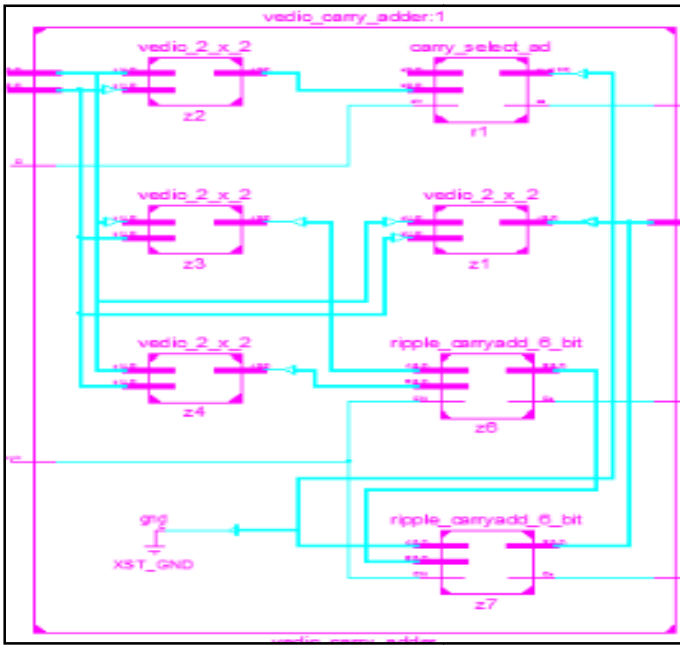

Fig.7 RTL view of Vedic multiplier using Urdhva Tiryakbhyam

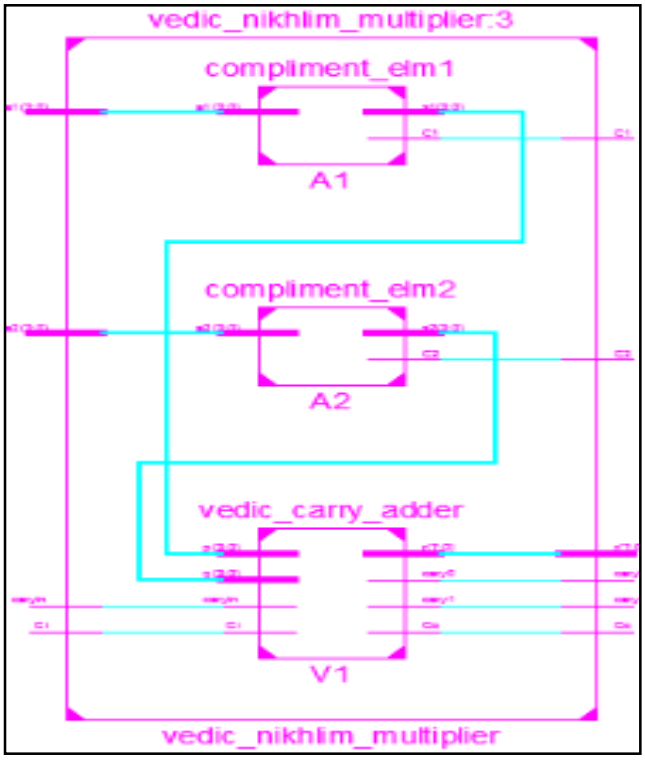

Fig.8 RTL View of Nikhilam Vedic Multiplier

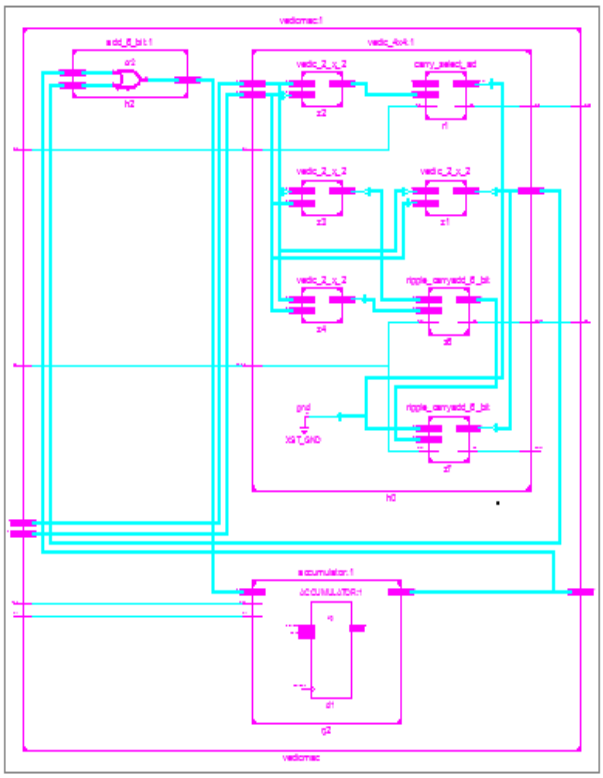

Fig.9 RTL View of MAC unit

5. SYNTHESIS RESULT

Table 1.

Logic Utilization	Used	Available	Utilization
Number of Slices	22	960	2%
Number of 4 input LUTs	8	1920	2%
Number of IOs	22	-	-
Number of bonded IOBs	22	66	33%

Table 2. Comparison table

Device: XC3S500/ XC3S1600, Xilinx Spartan3E(Family)	ARRAY MULTIPLIER	BOOTH MULTIPLIER	CONVENTIONAL VEDIC MULTIPLIER	VEDIC MULTIPLIER USING CARRY SELECT ADDER
4X4 Bit	32.001	16.276	13.182	11.764

6. CONCLUSION AND FUTURE WORK

A unique approach is proposed in this thesis to reduce the delay of MAC Unit using Vedic multiplier that is used CSLA architecture. This thesis shows the design of MAC using Vedic multiplier implemented by carry select adder compared with regular multiplier and modified 4X4 vedic multiplier. All these adder and multiplier and MAC unit are implemented on Spartan XC3S500E device and Xilinx 13.4 version. Also the RTL structure was analyzed using synopsis RTL tool. This diagram having better results when compared to conventional multiplier and modified techniques. The main area of VLSI is to reduce the area and delay. In this proposed topic we have to reduce the delay. Now to work on efficient area is the future work of this proposed topic.

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